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## **Simulation And Debug Of Mixed Signal Virtual Platforms For ...**

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Simulation and Debug of Mixed Signal Virtual Platforms for Hardware-Software co-development. Vincent Motel, Cadence Design Systems, Inc. (vmotel@cadence.com) Alexandre Roybier, Cadence Design Systems, Inc. (aroybier@cadence.com) Serge Imbert, Cadence Design Systems, Inc. (sergeim@cadence.com) Abstract—Virtual platforms are often used for high level architecture exploration and hardware-software interactions verification.

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Proteus Virtual System Modelling (VSM) blends mixed-mode SPICE simulation with world leading fast microcontroller simulation. It enables rapid prototyping of both hardware and firmware designs, in software. Design, Test and Debug your embedded projects in the Proteus electronic circuit simulator before a physical prototype is ordered.

### **Microcontroller Co-simulation | Edasim**

Simulink ® supports debugging with Simulation Stepper, which

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lets you step back and forth through your simulation. Use the Simulation Stepper to view data and inspect how and when the system changes states. For information, see How Simulation Stepper Helps With Model Analysis.. Simulink also includes the Simulink Debugger, which, like the Simulation Stepper, also enables you to start, stop ...

### **Test and Debug Simulations - MATLAB & Simulink**

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Mixed HDL Simulation. ModelSim combines simulation performance and capacity with the code coverage and debugging capabilities required to simulate multiple blocks and systems and attain ASIC gate-level sign-off. Comprehensive

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support of Verilog, SystemVerilog for Design, VHDL, and SystemC provide a solid foundation for single and multi-language design verification environments.

### **ModelSim ASIC and FPGA Design - Mentor Graphics**

The Questa Advanced Simulator is the core simulation and debug engine of the Questa Verification Solution; the comprehensive advanced verification platform capable of reducing the risk of validating complex FPGA and SoC designs. ... improving SystemVerilog and mixed VHDL/SystemVerilog RTL simulation performance by up to 10X. Questa also ...

### **Questa Advanced Simulator - Mentor Graphics**

Hence, setting up proper simulation options is very crucial in AMS debugging. For user friendly debugging, the simulation must be run with debug switch enabled in the simulation control file( spectre.scs). Typical example of such using Spectre®

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simulator is shown below. Figure 8 Specre debugging options. From the above example,

### **Debugging of Mixed Signal SoC in an effective and ...**

SimVision Debug can be used to debug digital, analog, or mixed-signal designs written in Verilog, SystemVerilog, e, VHDL, and SystemC ® languages or a combination thereof. SimVision integrated debug supports signal-level and transaction-based flows across all IEEE-standard design, testbench, and assertion languages, in addition to concurrent visualization of hardware, software, and analog domains.

### **SimVision Debug - Cadence**

Simulink also supports debugging with the Simulation Stepper, which lets you step back and forth through your simulation, viewing data and inspecting how and when the system changes states. For information, see [How Simulation Stepper Helps With](#)



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Model Analysis .

## **Simulink Debugger - MATLAB & Simulink - MathWorks France**

Synopsys' Verdi® Advanced AMS Debug provides comprehensive views of the overall design and enables seamless debug for co-simulation of analog, digital and mixed-signal subsystems within a unified debug environment.

## **Verdi Advanced AMS Debug - Synopsys**

simulation through the support of mixed-signal behavioral languages (verilog.ams) • Deals with schematics and text netlists

- Encompasses environment for simulation and debugging
- Supports both analog and digital centric methodology
- Has three usage models -Analog Design Environment (ADE)
- Hierarchy Editor (HED) -Command line

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## **Analog Mixed-Signal Simulation Results with Cadence Hierac**

The original Modeltech (VHDL) simulator was the first mixed-language simulator capable of simulating VHDL and Verilog design entities together. In 2003, ModelSim 5.8 was the first simulator to begin supporting features of the Accellera SystemVerilog 3.0 standard.

## **List of HDL simulators - Wikipedia**

The combination of CustomExplorer Ultra and Synopsys' CustomSim™/VCS® mixed-signal verification solution provides design teams with a high-performance, productive mixed-signal simulation and regression management environment for complex system-on-chip (SoC) verification.

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